THAT WHICH IS CLAIMED IS:

1. A flash memory device, comprising:

an address compare circuit that is configured to indicate whether an applied row address associated with a first operation is within or without an unlock area of a flash memory array, said applied row address having a most significant bit that operates as a chip select signal that is received by said address compare circuit; and

a control circuit that is configured to block performance of the first operation on the flash memory array in response to detecting an indication from said address compare circuit that the applied row address is without the unlock area of the flash memory array.

2. The flash memory device of Claim 1, wherein said address compare circuit comprises:

a start address register that is configured to latch an applied start row address in-sync with a start clock signal; and

an end address register that is configured to latch an applied end row address in-sync with an end clock signal.

3. The flash memory device of Claim 2, wherein said address compare circuit further comprises:

a start address comparator that is configured to receive a latched start row address from said start address register; and

an end address comparator that is configured to receive a latched end row address from said end address register.

4. The flash memory device of Claim 3, wherein said start address comparator comprises boolean logic that is configured to perform a comparison between the latched start row address and the applied row address; and wherein said end address comparator comprises boolean logic that is configured to perform a comparison between the latched end row address and the applied row address.

5. The flash memory device of Claim 4, wherein said address comparator is configured to generate an unlock signal that indicates whether the applied row address associated with the first operation is within or without the unlock area of the flash memory array.

6. The flash memory device of Claim 5, wherein said control circuit is responsive to the unlock signal.

7. The flash memory device of Claim 1, wherein said control circuit comprises:

a first clock generator having a pulse counter therein that is configured to generate a start clock signal in response to receipt of a plurality of consecutive address input pulses.

8. The flash memory device of Claim 7, further comprising a first address register that is configured to latch a start address of an unlock area in-sync with the start clock signal.

9. The flash memory device of Claim 1, wherein said control circuit comprises:

a first clock generator that is configured to generate a start clock signal in response to receipt of at least one address input pulse.

10. A flash memory device, comprising:

a flash memory array;

a word line control circuit electrically coupled to word lines in said flash memory array and responsive to a command control signal;

a bit line control circuit electrically coupled to bit lines in said flash memory array and responsive to the command control signal;

an address compare circuit that is configured to indicate whether an applied row address associated with a command is within or without an unlock area of said flash memory array, by generating an unlock signal at an active level if the applied row address is within the unlock area or at an inactive level if the applied row address is without the unlock area;

a primary control circuit that is configured to generate a command enable signal in response to the command and the unlock signal; and

a command control circuit that is configured to generate the command control signal in response to the command enable signal.

11. The flash memory device of Claim 10, wherein said primary control circuit is responsive to an address input pulse signal received at a pin of the flash memory device; and wherein the flash memory device is configured to latch first and second portions of the applied row address in-sync with first and second consecutive leading edges of the address input pulse signal.

12. The flash memory device of Claim 10, wherein said primary control circuit is further configured to generate a comparator reset signal in response to a leading edge of a reset signal received by the flash memory device; and wherein said address compare circuit is responsive to the comparator reset signal.

13. The flash memory device of Claim 10, wherein said address compare circuit comprises:

a start address register that is configured to latch an applied start row address in-sync with a start clock signal; and

an end address register that is configured to latch an applied end row address in-sync with an end clock signal.

14. The flash memory device of Claim 13, wherein said address compare circuit further comprises:

a start address comparator that is configured to receive a latched start row address from said start address register and the applied row address; and

an end address comparator that is configured to receive a latched end row address from said end address register and the applied row address.

15. The flash memory device of Claim 14, wherein said start address comparator comprises boolean logic that is configured to perform a comparison between the latched start row address and the applied row address; and wherein said end address comparator comprises boolean logic that is configured to perform a comparison between the latched end row address and the applied row address.

16. The flash memory device of Claim 13, wherein said primary control circuit is further configured to generate the start clock signal in response to a first sequence of address input pulses and generate the end clock signal in response to a second sequence of address input pulses.

17. A method of operating a flash memory device, comprising the steps of:

loading at least first and second portions of a start address associated with an unlock area of a flash memory array into the flash memory device, in-sync with respective ones of a first plurality of consecutive address input pulses;

loading at least first and second portions of an end address associated with the unlock area into the flash memory device, in-sync with respective ones of a second plurality of consecutive address input pulses;

loading at least first and second portions of an applied address associated with an erase or program command into the flash memory device, in-sync with respective ones of a third plurality of consecutive address input pulses; and

comparing the applied address with the start and end addresses to determine whether the erase or program command is to be performed on the unlock area.

18. The method of Claim 17, wherein said comparing step comprises evaluating whether the applied address is greater than or equal to the start address and evaluating whether the applied address is less than or equal to the end address.

19. The method of Claim 17, wherein said comparing step comprises generating an unlock signal having a first level that enables performance of the erase or program command and a second level that blocks performance of the erase or program command.

20. A method of operating a flash memory device, comprising the steps of:

loading a start row address associated with an unlock area of a flash memory array into the flash memory device;

loading an end row address associated with the unlock area into the flash memory device;

loading an applied row address associated with an erase or program command into the flash memory device;

comparing the applied row address to the start row address to determine whether the applied row address is greater than or equal to the start row address;

comparing the applied row address to the end row address to determine whether the applied row address is less than or equal to the end row address; and

generating an unlock signal at an active level in response to determining that the applied row address is greater than or equal to the start row address and less than or equal to the end row address.

21. A flash memory system, comprising:

a first flash memory chip comprising:

a first flash memory array;

a first address compare circuit that is configured to indicate whether an applied address associated with a first operation is within or without an unlock area of the first flash memory array; and

a first control circuit that is configured to block performance of the first operation on the first flash memory array in response to detecting an indication from said first address compare circuit that the applied address is without the unlock area of the first flash memory array; and

a second flash memory chip comprising:

a second flash memory array;

a second address compare circuit that is configured to indicate whether the applied address associated with the first operation is within or without an unlock area of the second flash memory array; and

a second control circuit that is configured to block performance of the first operation on the second flash memory array in response to detecting an indication from said second address compare circuit that the applied address is without the unlock area of the second flash memory array.

22. The flash memory system of Claim 21, wherein said first and second flash memory chips are mounted within a single integrated circuit package.

23. The flash memory system of Claim 21, wherein said first and second control circuits are responsive to a most significant bit of the applied address.

24. The flash memory system of Claim 23, wherein said first control circuit is selectively enabled when the most significant bit of the applied address equals a first logic value; and said second control circuit is selectively enabled when the most significant bit of the applied address equals a second logic value opposite the first logic value.